

Two-terminal Memory Devices Using Silicon Nano-structures

*Sattam Alotaibi, Konstantina Saranti, Shashi Paul**

Emerging Technologies Research Centre

De Montfort University, The Gateway, Leicester, LE1 9BH, United Kingdom

*E-mail: * spaul@dmu.ac.uk*

Summary: This work demonstrates the fabrication and investigation of a non-volatile memory on glass substrate using silicon (Si) nano-structures as the storage medium. Silicon nano-structures have appealing electrical and optical properties for their size and their uses have been demonstrated in a wide range of electronic applications.

The two-terminal memory devices, discussed in this paper, have the following structure: bottom and top metal contacts, two dielectric layers and silicon nano-structures in between those layers as the storage element. Plasma enhanced chemical vapour deposition (PECVD) technique was used to deposit insulator layer and silicon nano-structures. Current-voltage (I-V), current-time (I-t) measurements were conducted and scanning electron microscopy (SEM) was used in order to investigate the memory behaviour. The memory effect is observed as the difference between two electrical conductivity states (Low “0” and high “1”).

Keywords: non-volatile memory, silicon nano-structures, PECVD, retention time

1. Introduction

In the last decades a rapid development in the field of electronic memory devices is observed. Non-volatile memories (NVM) are widely used to store data because they can retain their state with no power supply. Flash memory is a type of NVM. Nowadays, there is an increasing demand for electronic devices. This has led to further research into flash memory devices with an aim to fabricate reliable and much higher density memory chips. The main aim of this work is to investigate the possibility of using silicon nano-structures to fabricate two-terminal electronic memory devices. The use of nano-structures will improve the reliability and density of the memory chip, thus the ability to store more information for a longer period of time (>10 years).

Mih et al have conducted an interesting study of silicon nano-structure incorporation in non-volatile memory devices. The study was based on low temperature deposition techniques for nano-structures fabrication [1, 2]. This paper aims to further investigate and provide a discussion of the use of silicon nano-structures as an alternative data storage element in non-volatile memory devices.

2. Experimental

In this experiment, we used a glass substrate that was thoroughly cleaned by decon, de-ionised water, acetone and isopropyl alcohol. Once the cleaning process was completed, 200 nm aluminium (Al) tracks were deposited by thermal evaporation. Following this, PECVD method was used in order to deposit the dielectric layer of 20 nm of Si₃N₄ (silicon nitride). The silicon nitride film was grown using silane (SiH₄), ammonia (NH₃) and nitrogen (N₂) with a chamber pressure of 350 mTorr, radio frequency (RF) power of 20 Watts at 300°C deposition temperature. The substrate underwent an initial preparation step (details of the precise procedure and material will be published elsewhere) that enables the growth of silicon nano-structures at low temperatures. The coated substrate was then placed in PECVD chamber and silicon nano-structures were grown using gas mixture of SiH₄ and H₂ (hydrogen), chamber pressure 200 mTorr, RF power 250 Watts, growth temperature 400°C and 30 minutes growth time. Following this, another dielectric film of Si₃N₄ was deposited on top of the silicon nano-structures with the same growth conditions as described for the first Si₃N₄ layer. Finally, in order to complete the structure of the device, 100 nm thick Al tracks (top contacts) were deposited using thermal evaporator. For electrical measurements, we used a PC-driven pico ammeter (HP4140B) and LCR bridge (HP4192) with impedance of 1 MHz. The electrical measurements were carried out at room temperature in an e-m (electromagnetic) shielded dark box.

3. Results and Discussion

The schematic diagram of a two-terminal memory device structure is shown in Fig-1(a). The device configuration is as follows: glass substrate / Al / Si₃N₄ / Si nano-structures / Si₃N₄ / Al. Fig.-1(b) is an SEM image of the silicon nano-structures used as a medium for storing electronic information.

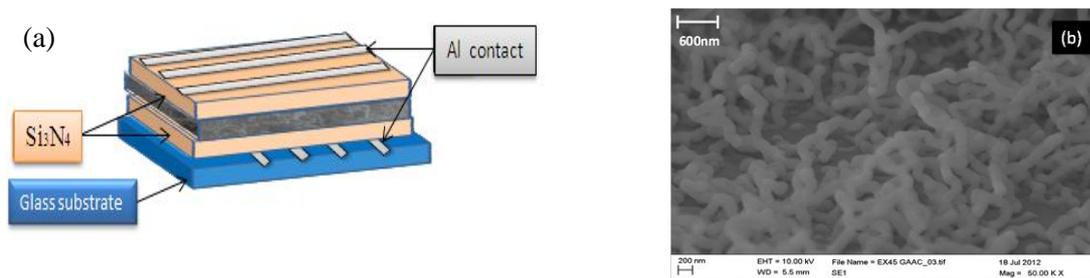


Fig.1. (a) Schematic structure of two-terminal memory device using silicon nanostructures. The device has the simple structure of silicon nanostructures sandwiched between dielectric layers (Si₃N₄) on glass substrate with aluminium bottom and top contacts, (b) SEM image of silicon nano-structures grown by PECVD technique with an average diameter of 140 nm.

A current voltage (*I-V*) characteristic of the memory device is shown in Fig.2 (a) and the hysteresis in the electrical behaviour is an indication of charge storage in the nano-structures. The devices were fabricated without the initial preparation step, which means no nano-structures but a layer of amorphous silicon; do not show any appreciable hysteresis. Fig.2 (b) shows two different electrical conductivity states for the two-terminal memory device. By applying +40V to the device, followed by a read voltage of +25V, the device is switched to the high conductivity state, namely “0”. Then this high state was switched to the low conductivity state “1” by applying -40V and read at the same voltage of +25V. It is obvious from Fig.2 (b) that around 60% of the charge was lost within the first 20 seconds. After that, it stayed mainly constant with around 100 pA difference.

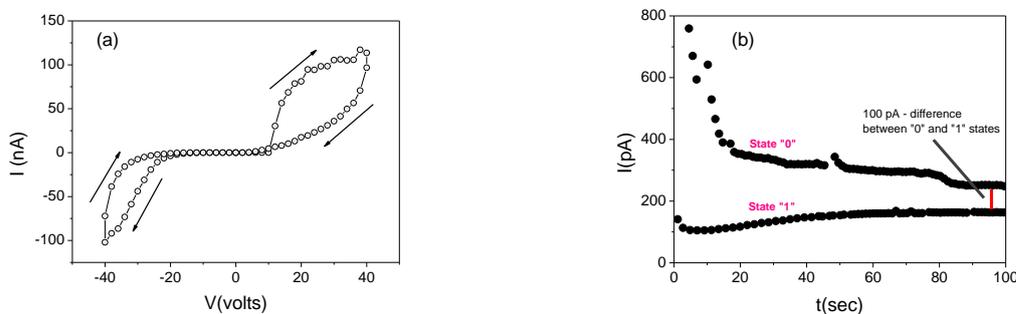


Fig.2.(a) *I-V* characteristics of two-terminal memory devices. The charge storage is reflected in the hysteresis in *I-V* behaviour. (b) Data retention characteristic of the same two-terminal memory device for 100 pulses. It is noticed that 60% of the charge was lost in the first few pulses but afterward a discernible difference (100 pA) is maintained between two conductance states.

4. Conclusion

In this paper, the fabrication and analysis of a non-volatile memory device on glass substrate is presented. It is shown that silicon nano-structures have the potential to be used as a storage medium for two-terminal non-volatile memory devices. The charge storage is observed from the hysteresis of the *I-V* characteristic while two distinguishable electrical conductivity states (“0” and “1”) are shown by the *I-t* data.

5. References

- [1] T.A. Mih, R.B. Cross, and S. Paul., “A novel method for the growth of low temperature silicon structures for 3-D flash memory devices,” Materials Research Society Symposium Proceedings, 1112, (2009), 265-269.
- [2] T.A. Mih, "A Novel Low-Temperature Growth Method of Silicon Structures and Application in Flash Memory", Ph.D dissertation., Leicester: De Montfort University,(2011), 62.