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To whom it may concern:

This is to certify that Mr Mohammed Aqeeli, from University of Manchester , attended and presented his paper entitled "Low-Phase Noise Variation VCO Implementing Resistorless Digitally Controlled Varactor" at the ICICDT conference, at imec, Belgium,

Sincerely,

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Low-Phase Noise Variation VCO Implementing Resistorless Digitally Controlled Varactor

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***Abstract*—A novel resistorless digital capacitor switching array (DCSA) has been implemented into a wideband CMOS VCO for 5-GHz WiMAX/WLAN applications. The proposed DCSA is added both in series and parallel to nMOS varactors. Based on this, a wideband VCO is achieved, which not only exhibits lower phase noise in comparison with reported state-of the- art wideband VCOs, but also has low phase noise variation of less than 5 dBc/Hz. In addition, it has demonstrated low power consumption, improved linearity of the f-V curve and extended tuning range. The proposed VCO has been designed using UMC 130 nm CMOS technology. It operates from 3.65 GHz to 6.34 GHz, with a phase noise of -132.70 dBc/Hz at 1 MHz offset, a figure of merit (FoM) of -202.9 dBc/Hz, less than -41 dBm spurious harmonics and total VCO core power consumption of 2.88 mW from a 3.2 V supply voltage.**

Keywords*— *CMOS; phase noise variation, VCO gain, tuning range, figure of merit.

I. INTRODUCTION

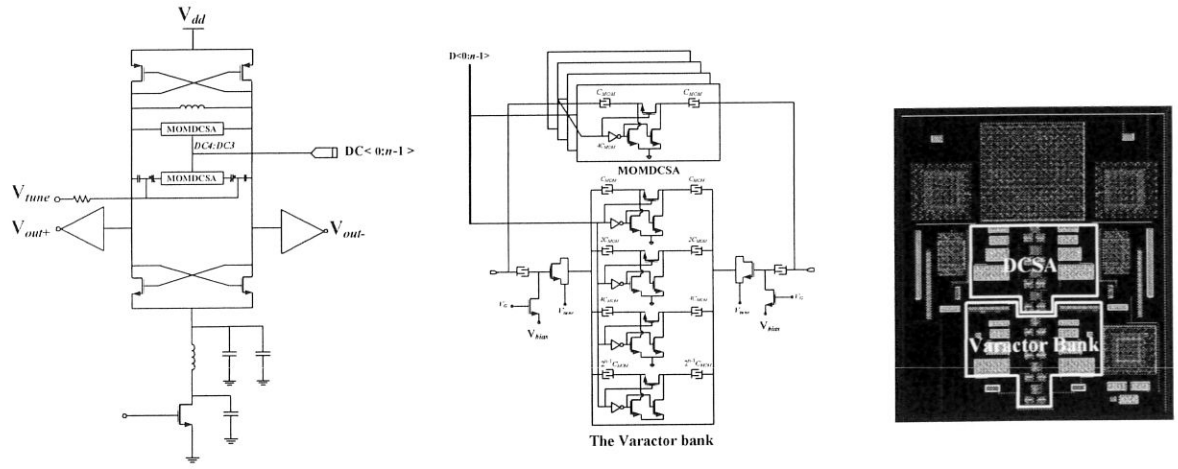
Phase noise can vary dramatically over the tuning range of a VCO, but the published literature often overshadow this problem by measuring or simulating phase noise at the center frequency only[1]. It is difficult to obtain simultaneously a large tuning range and small phase noise variation, particularly while accommodating MOS or diode varactors. Using a MOS transistor as a varactor increases the probability of converting AM noise to FM noise[2]. This will grow in line with the difference between the maximum and the minimum capacitances and may become indistinguishable from phase noise. Consequently, when the tuning range is more than 30 percent, switching capacitors are mandatory to maintain minimum phase noise variations, tuning linearity and low VCO sensitivity[3]. Studies have been conducted which consider switching capacitors inside the LC tank in order to extend the tuning range and improve VCO phase noise. However, these studies used switches that were implemented using stacked devices and large resistors to gain high impedance for RF signals, resulting in occupying a larger die area as well as exhibiting higher power dissipation and phase noise. This article presents a novel VCO which consists of two sets of high-performance 4-bit digital capacitor switching arrays (DCSA) added both in series and parallel to nMOS varactors. Such an approach enables the VCO to have an extended tuning bandwidth and minimizes the phase noise variation throughout the entire tuning range, while maintaining minimum die size. Previous resistors employed[4][5][6] have been replaced with much smaller nMOS transistors, which perform as resistors. These in turn occupy a much smaller area, resulting in less parasitic capacitance affecting the RF nodes of the VCO. As a result, the proposed VCO has many advantages, such as providing a solution to the problem of high phase noise variation associated with wideband tuning, and minimizing the sensitivity of the VCO by optimizing gain. Finally, it has an output frequency which varies linearly with the control voltage. The proposed VCO's bandwidth is increased by more than 6 percent, phase noise has decreased by more than 12.7 dBc/Hz, and phase noise variation is less than 4.9 dBc/Hz in comparison with most recently reported works. This paper is organized as follows: Section II explains the VCO's core design and the implementation process, Section III presents the resonator tank design, Section IV illustrates the varactor characterization and simulation results, followed by the conclusion in Section V.

II. CIRCUIT DESIGN AND IMPLEMENTATION

A complementary cross-coupled VCO based on a binary-weighted switched capacitor bank and nMOS varactors is depicted in Fig. 1(a). This topology is chosen due its ability to achieve lower phase noise when compared to other configurations. The LC tank consists of a differentially-tuned varactor group and a very small, symmetrical, center-tapped inductor. A cross-connected differential pair provides negative resistance to neutralize the tank losses; this results in less current consumption and is thus more power-efficient. The wider the tuning bandwidth, the higher the phase noise, this means an RF VCO with sub-bands is the best choice for broadband implementation. Equation (1) shows clearly that the phase noise of the VCO is proportional to the square of the VCO gain[10].

$$S_{\phi n} = \left(\frac{K_{VCO}}{S} \left| Z(\omega_0 + \Delta\omega_0) \right| \right)^2 \cdot \bar{i}_n^2 . \alpha \frac{1}{Q^2} \left(\frac{K_{VCO}}{2\Delta\omega_0} \right)^2 \quad (1)$$

where K_{VCO} is the gain of the VCO, ω_0 is the carrier frequency, $\Delta\omega_0$ is the offset frequency, i_n is the noise current Q is the quality factor of the LC tank. In order to obtain low phase noise, low K_{VCO} is necessary. Furthermore, to minimize phase noise variation, the K_{VCO} must be minimized and remain



(a) (b) (c)

Fig. 1. (a) Schematic diagram of the proposed 5.0 GHz 130 nm CMOS VCO. (b) DCSA and its logic control with varactor bank. (c) Layout of the VCO with a die area of 720× 586 μm2.

constant across the tuning range. This means that the oscillation frequency will vary linearly with the tuning voltage.

III. Novel Varactor for Low Phase Noise Variation

Apart from wideband tuning range performance, it is highly desirable for a VCO to provide constant phase noise across its operating frequency range, or at least to maintain an acceptable phase noise variation for all frequencies[11]. To achieve a wide tuning range for lower phase noise and minimum variation, two sets of DCSA are used in the proposed VCO. The first one is in series with the nMOS varactors, and the second is in parallel with the inductor as depicted in Fig. 1(b), to divide the tuning range into multiple frequency bands. The nMOS transistors occupy a smaller die area compared to pMOS transistors, and thus fewer parasitic capacitances are added to the VCO core. Such an arrangement will extend the linear tuning range of the varactors and importantly reduce the K_{VCO}, phase noise and phase noise variation[11]. It was found that this topology provides a relatively constant output swing frequency and minimal phase noise over the operating frequency range. Consequently, phase noise variation challenges are optimized. The operation of the DCSA was implemented using symmetric-type MOM capacitors, because of their large capacitance, low parasitic capacitance, symmetrical plate design, superior RF characteristics and their requirement of no additional masks or process steps[10][11]. In order to reduce phase noise variations we had to find the VCO design parameters which could compensate for the K_{VCO} variations. The DCSA capacitance value can be calculated as:

$$C = (2^{N-1})\left(\frac{1}{C_{MOM}} + \frac{1}{C_{DF}}\right)^{-1} \tag{2}$$

where C_{MOM} is the capacitance of the DCSA, and CDF is the drain fringe capacitance of the switch devices. Total capacitance Cα of the series MOMDCSA, including fixed parasitic capacitance of the active devices, C_{par} can be calculated as:

$$C_{\alpha} = (2^{N-1})\left(\frac{1}{C_{MOM}} + \frac{1}{C_{DF}}\right)^{-1} + C_{PAR} \tag{3}$$

where C_{DF} is the drain fringe capacitance of the series MOMDCSA. Total capacitance C_{β} of the parallel MOMDCSA to the inductor and C_{α} is:

$$C_{\beta} = (2^{N-1})\left(\frac{1}{C_{MOM}} + \frac{1}{C_{DF\beta}}\right)^{-1} \tag{4}$$

where $C_{DF\beta}$ is the drain fringe capacitance of the parallel MOMDCSA. Total capacitance C_{γ} of the nMOS varactor and the series MOMDCSA can be calculated as:

$$C_{\gamma} = \frac{C_{\alpha}.C_{Var}}{C_{\alpha} + C_{Var}} \tag{5}$$

where C_{var} is the capacitance of the nMOS varactor

$$C_{\tan k} = \frac{C_{\alpha}.C_{Var}}{C_{\alpha} + C_{Var}} + C_{\beta} \tag{6}$$

The oscillation frequency (f_{osc}) of the VCO can be written as follows:

$$f_{Osc} = \frac{1}{2\pi\sqrt{L[(C_{\alpha}.C_{Var}/C_{\alpha} + C_{Var}) + C_{\beta}]}} \tag{7}$$

K_{VCO} can be derived as follows:

Assuming,

$$C_{\delta} = \frac{C_{Var}(C_{\alpha} + C_{\beta}) + C_{\alpha}.C_{\beta}}{C_{\alpha} + C_{Var}} \tag{8}$$

then,

$$K_{VCO} = \frac{\partial f_{Osc}}{\partial V_{Cont}} = -\frac{C_\alpha^{\,2}}{4\pi\sqrt{L}.C_\delta^{\,3/2}} \cdot \frac{1}{(C_\alpha + C_{Var})^2} \cdot \frac{\partial C_{Var}}{\partial V_{Cont}} \tag{9}$$

where V_{cont} is the controlled voltage. From (7), we have,

$$C_\delta = \frac{1}{4\pi^2.f_{Osc}^{\,2}.L} \tag{10}$$

Substituting (10) into (9) we obtain,

$$|K_{VCO}| = 2\pi^2.f_{Osc}^{\,3}.L.\frac{C_\alpha^{\,2}}{(C_\alpha + C_{Var})^2} \cdot \frac{\partial C_{Var}}{\partial V_{Cont}} \tag{11}$$

Equation (11) shows the third-order exponential relationship between the K_{VCO} and the frequency of oscillation. It demonstrates that the gain of the proposed VCO is a function of the LC tank.

IV. Characterisation and Simulation

The proposed VCO was implemented using a commercially available UMC 130 nm, 6-metal, mixed-mode CMOS process and simulated using Cadence Virtuoso analogue design environment tools (CVADET). Fig. 1(c) shows the layout of the proposed VCO which has a die area of 720× 586 µm2, not including the bond pad. To verify the proposed theory, two VCOs were designed, the first one with DCSA connected in parallel to the varactor bank while the second one has DCSA connected in both series and parallel to the varactor bank, the phase noise variation and VCO gain of the proposed VCO are simulated as a function of the control code of the switchable capacitor bank, while the varactor tuning voltage is fixed at 1.0 V. As can be seen, the first VCO shows a gain sensitivity of 23.5MHz/V and phase noise variation of 12.7 dBc/Hz as shown in Fig. 3. The proposed VCO resulting in better simulated performance in terms of K_{VCO}, which reduced to 5.7MHz/V and phase noise variation which was less than 4.9 dBc/Hz, as shown in Fig.4. As a result, the new varactor achieves steep transition for tuning voltages varying between 0 and 2.5 V. This steep transition occurs similarly at all tuning curves. After completing the physical design (layout), both design rule check (DRC) and layout versus schematic (LVS) check was performed using the Cadence tools. Parasitic capacitances and resistances in the layout were strongly affecting the performance of the proposed VCO. To evaluate the effects of parasitic and to gain a higher degree of confidence, Cadence quantus extraction tool (QRC) was used because it provides a convenient and accurate methodology to predict the performance in critical building blocks such the proposed LC-tank VCO. Simulating the design with parasitic capacitances and resistances accounted for, the phase noise was increased from -136.9 dBc/Hz to -132.7 dBc/Hz at 1MHz offset frequency. The simulation results indicate that the VCO exhibits a wider tuning range between 3.65 GHz and 6.34 GHz. Phase noise variations range from -136.34 dBc/Hz to -132.56 dBc/Hz and FoM varies from -202.1 dBc/Hz to -204.8 dBc/Hz at 1 MHz offset frequency. The new varactor achieves steep transition for tuning voltages, as depicted in Fig. 2.

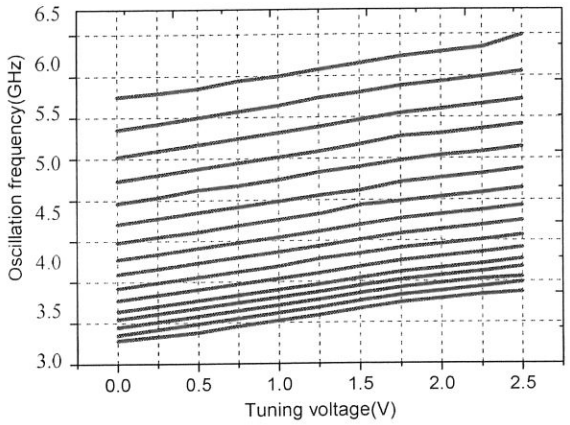


Fig. 2. Oscillation frequency characteristics versus tuning voltage.

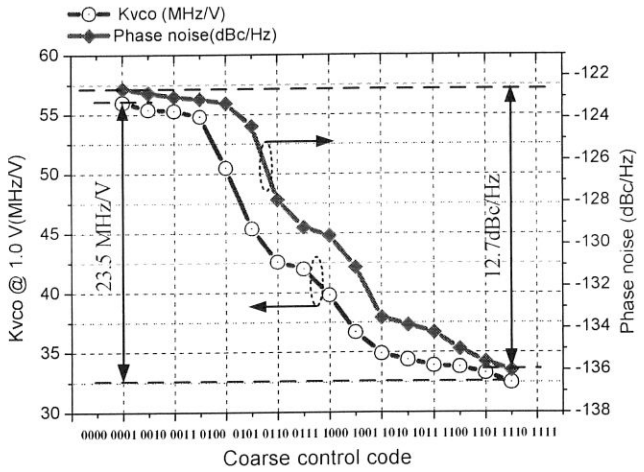


Fig. 3. VCO gain and phase noise of the proposed VCO with DCSA connected in parallel to the varactor bank.

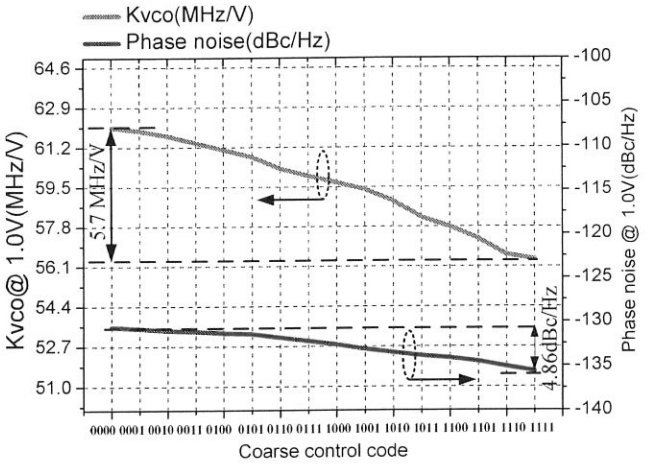


Fig. 4. VCO gain and phase noise of the proposed VCO with DCSA connected in series and in parallel to the varactor bank.

The proposed VCO has better performance parameters, due mainly to the MOMDCSA and the characteristics of the new topology. Importantly, phase noise variations remain relatively small for all tuning ranges, due to the advantages of the

Table I: Performance comparison of CMOS VCOs

Process	F (GHz)	P (mW)	PN (dBc/Hz)	Offset	TR (GHz)	FoM (dBc/Hz)	Ref.
0.18μmCMOS	5.00	7.20	-90.2	1.0	4.10-5.00	-154.80	[4]
0.18μmCMOS	4.20	4.50	-119.0	1.0	4.10-4.80	-184.47	[6]^S
0.18μmCMOS	5.00	13.00	-121.5	1.0	5.10-5.36	-192.10	[9]^S
0.18μmCMOS	3.50	8.80	-125.9	1.0	3.05-3.92	-191.70	[10]
0.18μmCMOS	5.80	10.08	-117.0	1.0	5.27-6.41	-184.00	[11]
0.09μmCMOS	3.95	6.60	-147.0	10.0*	3.40-4.50	-191.00	[12]
0.13μmCMOS	5.00	2.88	-132.7	1.0	3.65-6.34	-202.90	This work

F: Centre frequency, P: power, PN: Phase noise at 1 MHz, *at 10 MHz offset TR: Tuning range, FoM: Figure of Merit, S: Simulation

discrete frequency ranges. The topology of this VCO can be used for the implementation of local oscillator (LO) synthesizers in WLAN radio applications. Circuit performance, which was simulated using CVADET to show the transient analysis of the VCO, demonstrates clearly that steady-state oscillation starts at approximately 6.27 ns. The circuit generates stable periodic signals with a harmonic index and measured output power of approximately 3.73 dBm at the resonant frequency, with tuning voltage varying from 0 to 2.5 V. The FoM model adopted by Ham and Hajimiri[8] normalizes measured phase noise with respect to center frequency and power consumption, as shown by equation (12):

$$FOM = L\{\Delta f\} - 20\log\left\{\frac{f_0}{\Delta f}\right\} + 10\log\left\{\frac{P_d}{1mW}\right\} \qquad (12)$$

where $L\{\Delta f\}$ is the phase noise at offset frequency Δf, f_0 is the oscillating frequency, and P_d (W) is the power dissipation of the VCO. The performance of the novel VCO in this study is compared in Table I to other state-of-the-art designs in 0.09 μm, 0.13 μm and 0.18 μm CMOS technologies. It is evident that the proposed VCO has better characteristics with regard to phase noise, power consumption and FoM.

V. Conclusion

Using a novel design, a wideband LC-VCO has been designed and simulated to meet Wi-MAX/WLAN specification and the most stringent phase noise requirements. An ideal VCO has a broadband tuning range of approximately 49.2 per cent which varies linearly with the control voltage. The high performance VCO specifications include simulated phase noise of -132.7 dBc/Hz at an offset frequency of 1 MHz away from the 5.0 GHz FoM of -202.9 dBc/Hz, while the VCO core's total power consumption is 2.88 mW away from 3.2 V supply voltage. The proposed design is expected to be fabricated using multi-projects wafer fabrication in the near future.

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